WHAT IS CLAIMED IS:

1. A semiconductor test system for testing semiconductor devices, comprising:

a tester hardware for providing power sources to power source pins of a semiconductor device under test (DUT) and applying a test pattern to an input pin of the DUT and evaluating an output signal of the DUT;

a host computer operated by a general purpose operating system for controlling an overall operation of the semiconductor test system based on a test program;

a configuration software for computing configuration data indicating configuration of the power sources and reference voltages of the test pattern and timing data indicating timings of activating and deactivating the power sources, reference voltages and test pattern, the configuration software computing the configuration data and timing data based on the test program prior to testing the DUT;

a device driver for providing a power trigger and a signal trigger to the tester hardware to trigger the timings of activating and deactivating the power sources and the reference voltages in the hardware tester; and

a hardware timer for producing an interrupt signal after a predetermined time defined by the device driver and sending the interrupt signal to the device driver through the host computer;

wherein the device driver causes to start the test pattern upon receiving the interrupt signal from the hardware timer and to deactivate the power sources to the DUT upon receiving the interrupt signal from the hardware timer.

2. A semiconductor test system as defined in Claim 1, wherein the device driver causes to stop the test pattern upon receiving an end of test signal generated by the tester hardware through the host computer and triggers the hardware

timer to produce an interrupt signal after a specified time interval and causes to deactivate the power sources to the DUT upon receiving the interrupt signal from the hardware timer.

3. A semiconductor test system as defined in Claim 1, wherein the device driver is a software configured to respond to the interrupt signal through the host computer in a timely fashion with a minimal time latency and with high priority.

4. A semiconductor test system as defined in Claim 1, wherein the device driver is designed to respond to the interrupt signal generated by the hardware timer or an interrupt signal generated by the tester hardware.

5. A semiconductor test system as defined in Claim 1, wherein the tester hardware includes a hardware control circuitry for formatting the test pattern based on the reference voltages defined by the configuration data from the configuration software and for forming the power sources for the DUT defined by the configuration data from the configuration software.

6. A semiconductor test system as defined in Claim 5, wherein the tester hardware further includes a comparator for comparing the output signal of the DUT with an expected signal and producing a failure signal when detecting mismatch between the output signal and the expected signal, and an end of test logic for producing an end of test signal when receiving the failure signal from the comparator.

7. A semiconductor test system as defined in Claim 6, wherein the host computer produces an interrupt signal upon receiving the end of test signal from the tester hardware and provides the interrupt signal to the device driver.

8. A semiconductor test system for testing semiconductor devices, comprising:

a tester hardware for providing power sources to power source pins of a semiconductor device under test (DUT) and applying a test pattern to an input pin of the

DUT and evaluating an output signal of the DUT;

a host computer operated by a general purpose operating system for controlling an overall operation of the semiconductor test system based on a test program;

means for computing configuration data indicating configuration of the power sources and reference voltages of the test pattern and timing data indicating timings of activating and deactivating the power sources, reference voltages, and test pattern wherein the configuration data and timing data are determined based on the test program prior to testing the DUT;

means for providing a power trigger and a signal trigger to the tester hardware to trigger the timings of activating and deactivating the power sources and the reference voltages in the hardware tester; and

a hardware timer for producing an interrupt signal after a predetermined time defined by the providing means and sending the interrupt signal to the providing means through the host computer;

wherein the test pattern is started upon receiving the interrupt signal from the hardware timer and the power sources to the DUT is deactivated upon receiving the interrupt signal from the hardware timer.

9. A semiconductor test system as defined in Claim 8, wherein the test pattern ends upon receiving an end of test signal generated by the tester hardware, and the hardware timer produces an interrupt signal at a specified time after the end of test signal, and the power sources to the DUT are deactivated immediately after the interrupt signal from the hardware timer.

10. A semiconductor test system as defined in Claim 8, wherein the tester hardware includes a hardware control circuitry for formatting the test pattern based on the reference voltages defined by the configuration data determined by the computing means and for forming the power

sources for the DUT defined by the configuration data determined by the computing means.

11. A semiconductor test system as defined in Claim 8, wherein the tester hardware further includes a comparator for comparing the output signal of the DUT with an expected signal and producing a failure signal when detecting mismatch between the output signal and the expected signal, and an end of test logic for producing an end of test signal when receiving the failure signal from the comparator.

12. A semiconductor test system as defined in Claim 8, wherein the host computer produces an interrupt signal upon receiving the end of test signal from the tester hardware.